2. (Once Amended) The multi layer integrated circuit capacitor of claim 1 further comprising a plurality of controlled collapse chip connection (C4) lands fabricated on and contacting the third insulator layer and in electrical contact with the plurality of conductive vias.

9. (Twice Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer, the second conductive layer being fabricated as a plurality of laterally spaced strips such that a surface area of the second conductive layer is less than a surface area of the first conductive layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer, the third conductive layer being fabricated as a plurality of laterally spaced strips such that a surface area of the third conductive layer is less than the surface area of the second conductive layer;

a third insulator layer located over the third conductive layer;

a first plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the third conductive layer;

a second plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the second conductive layer; and

a third plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first conductive layer.

11. (Twice Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer;

a first plurality of conductive vias downwardly extending through the third insulator layer, the third conductive layer, the second insulator layer, the second conductive layer and the first insulator layer to provide electrical interconnection to the first and third conductive layers; and

a second plurality of conductive vias downwardly extending through the third insulator layer, the third conductive layer, and the second insulator layer to provide electrical interconnection to the second conductive layer.

14. (Twice Amended) A circuit board assembly comprising:

a circuit board having a pair of supply voltage interconnect lines;

a first integrated circuit die mounted on the circuit board and electrically connected to the supply voltage interconnect lines; and

a second integrated circuit die mounted on the circuit board and electrically connected to the supply voltage interconnect lines, the second integrated circuit [package] <u>die</u> comprising a capacitor having:

a substrate;

a first conductive layer located over <u>and contacting</u> the substrate;

a first insulator layer located over <u>and contacting</u> the first conductive layer, <u>the first insulator layer not contacting the substrate;</u>

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers.

15. (Once Amended) The circuit board assembly of claim 14 wherein the second integrated circuit [package] die comprises a plurality of controlled collapse chip connection (C4) lands that are electrically connected to the plurality of conductive vias and the supply voltage interconnect lines.

19. (Twice Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second, and third conductive layers, the plurality of conductive vias further extending through the substrate to provide electrical interconnection to both a top surface and a bottom surface of the integrated circuit capacitor.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on November 7, 2001, and the references cited therewith. Claims 1, 2, 9, 11, 14, 15, and 19 are amended, no claims are canceled, and no claims are added; as a result, claims 1-21 are now pending in this application.

Rejections Under 35 U.S.C.§102

Claims 1, 2, 14-16, and 19 were rejected under 35 U.S.C.§102(e) as being anticipated by Farooq et al. (U.S. Patent No. 6,072,690); claims 1, 8, and 11 were rejected under 35 U.S.C.§102(e) as being anticipated by Naito et al. (EP 0,917,165 A2); and claims 1, 7, and 9